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REED SMITH LLP
3110 FAIRVIEW PARK DRIVE, SUITE 1400
FALLS CHURCH, VA 22042

EXAMINER	
LEE, CHUN KUAN	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 05/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,602	TANAKA ET AL.	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Supervisory FRITZ FLEMING PRIMARY EXAMINER GROUP 2100 AU 2181 5/8/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, filed on 02/22/2006, with respect to claims 1-8 and 11 have been considered but are moot in view of the new ground(s) of rejection. Applicant's arguments with respect to claims 9-10 and 12-18 have been fully considered but they are not persuasive. It appears applicant's argument does not universally applied to all claims as amendments correlated to applicant's arguments are made only to certain claims, please see details below. Objections of claims 2, 5, 6, 10-12 and 17 and rejections of claims 3-4 under 35 U.S.C. § 112 are withdrawn. Currently claims 1-18 are pending for examination.

2. In responding to applicant's argument regarding the rejection to claim 1 under 35 U.S.C. § 102(e) that Stiffler shows that the storage device must be "dual-ported" and cannot be "single ported," therefore "dual ports" in Stiffler cannot be read on "a single port." Applicant's argument has been fully considered and was found not to be persuasive.

As reiterated in the independent claim 1, a computer system comprising a single port disposed in said I/O device and connected to said PCI bus, the claim is broad enough wherein it does not precluded for the computer system to have a plurality of one single port, wherein one of the plurality of single ports disposed in said I/O device and connected to said PCI bus. Further more, Stiffler teaches that the dual port can inherently be a single port if the storage device (disk array 616 of Fig. 6) is duplicated

with all disk stores initiated on the primary computer echoed by the second computer (col. 9, l. 52 to col. 10, l. 10). Stiffler shows the disk array (I/O device) (Fig. 6, ref. 616) comprising a port, wherein said port is connected to the PCI bus (Fig. 6, ref. 610, 624), wherein all disk stores initiated on the primary computer is echoed by the second computer, therefore said port comprises a single port.

3. In responding to applicant's argument regarding the rejection to claim 1 under 35 U.S.C. § 102(e) that Stiffler does not show one of the CPU is physically or logically taken off-line when an error occurs in that CPU and only one of the virtual machines, in which an error does not occur, can access the I/O device at a time. Applicant's argument has been fully considered and was found not to be persuasive.

Please note that the features upon which applicant relies (i.e., the CPU is physically or logically taken off-line when an error occurs in that CPU and only one of the virtual machines, in which an error does not occur, can access the I/O device at a time) are not recited in the rejected independent claim 1, as independent claim 1 does not appear to expressly recite the claim limitation regarding the occurrence of an error. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

4. In responding to applicant's argument regarding the rejection to claims 5, 13 and 16 under 35 U.S.C. § 102(e), wherein same arguments set forth in the arguments for

claim 1 is applicable. Applicant's argument has been fully considered and was found not to be persuasive.

As per claim 5, similar amendments made in claim 1 are also made in claim 5, therefore please see examiner's response as stated above for details and further more, claim 5 is moot in view of the new ground(s) of rejection.

As per claim 13 and 16, please note that similar amendments made in claim 1 are not made to claims 13 and 16, but the examiner's response set forth in claim 1 is applicable here. Please see examiner's response as stated above for details.

5. As per dependent claims 3 and 7, as claims 3 and 7 are dependent on independent claims 1 and 5 and therefore are unpatentabe at least because they include all the limitations recited in the independent claims 1 and 5, and furthermore, claims 3 and 7 are moot in view of the new ground(s) of rejection due to amendments made to claims 3 and 7.

6. As per dependent claims 15 and 17, as claims 15 and 17 are dependent on independent claims 13 and 16 and therefore are unpatentabe at least because they include all the limitations recited in the independent claims 13 and 16.

7. In responding to applicant's argument regarding the rejection to claim 2 under 35 U.S.C. § 103(a) that the "interrupt" in the presentation is different from that taught in "Computer Input/Output" because said interrupt provides interruption initiating a transfer

for a message that a control program has removed the disk unit to a firmware such as a BIOS or an operating system.

Please note that the features upon which applicant relies (i.e., interrupt initiating a transfer for a message that a control program has removed the disk unit to a firmware such as a BIOS or an operating system) are not recited in the rejected claim 2, as claim 2 recited the generated interrupt is to notify a change of the state of logical connection. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

8. As per dependent claims 4 and 8, as claims 4 and 8 are dependent on independent claims 1 and 5, please see examiner's response as stated above for details and further more, claims 1 and 5 are moot in view of the new ground(s) of rejection, therefore claims 4 and 8 are moot in view of the new ground(s) of rejection.

9. As per claims 6, 9, 12, 14 and 18, please see examiner's response as stated above set forth in claims 1 and 2 for details, as claims 6, 9, 12, 14 and 18 have substantially the same features as those of claims 1 and 2.

10. As per dependent claim 10, as claim 10 is dependent on independent claim 9 and therefore are unpatentabe at least because they include all the limitations recited in the independent claim 9.

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 13, 15 and 16-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Stiffler et al. (US Patent 6,622,263).

12. As per claim 13, Stiffler teaches a method for sharing an I/O device (disk array 616 of Fig. 6) connected to a PCI bus (Fig. 6, ref. 610, 624) of a computer among a plurality of virtual machines (Fig. 6, ref. 601, 603) formed on a control program of said computer, including:

a step of enabling said I/O device to set a state of logical connection between selected one of said plurality of virtual machines (secondary computer 603 of Fig. 6) (Fig. 6; Fig. 9 and col. 10, ll. 20-64) and a single port of said I/O device connected to said PCI bus through said single port (col. 9, l. 52 to col. 10, l. 10), wherein the disk array is duplicated by having all disk stored initiated on the primary computer echoed by the second computer therefore the disk array would inherently have the single port; and

a step of changing said state of logical connection between said port and said selected virtual machine according to a control signal received from said selected virtual machine (Fig. 9 and col. 10, ll. 20-64), wherein upon implementing the takeover control signal procedure by the secondary computer the logical connection between the disk

array and the secondary computer becomes active and the secondary computer becomes the new primary computer.

13. As per claim 15, Stiffler teaches the method further comprising:

wherein said step of changing said state of logical connection, when detecting error occurrence in any of said plurality of virtual machines (primary computer), inherently updates an allocation table for setting said state of logical connection between said port and each virtual machine, lets said error-detected virtual machine (primary computer) stand by (taken off-line) and activate another virtual machine (secondary computer) (col. 10, ll. 20-64 and col. 11, l. 51 to col. 12, l. 17), wherein when error occurrence is detected in the primary computer, the primary computer is taken off-line and the secondary computer is activated to become the new primary computer.

14. As per claim 16, Stiffler teaches a method for sharing an I/O device (disk array 616 of Fig. 6) connected to a PCI bus (Fig. 6, ref. 610, 624) of a computer among a plurality of virtual machines (Fig. 6, ref 601, 603) formed by partitioning said computer physically (Fig. 6, ref. 601, 603),

wherein said method includes:

a step of enabling said I/O device connected to said PCI bus through its single port to set a state of logical connection between selected one of said plurality of physical partitioned computers and said port (Fig. 6; Fig. 9 and col. 10, ll. 20-49), wherein the disk array is duplicated by having all disk stored initiated on the primary

computer echoed by the second computer therefore the disk array would inherently have the single port; and wherein if the primary computer fails, the state of logical connection between the primary computer and the disk array is deactivated as the primary computer will be taken off-line and the state of logical connection between the secondary computer and the disk array is activated as the secondary computer takes over to commence operating as the new primary computer; and

a step of changing said state of logical connection to said port according to a control signal received from said selected physical partitioned computer (Fig. 6; Fig. 9 and col. 10, ll. 20-49), wherein the state of logical connection between the secondary computer and the disk array becomes active as the secondary computer implement the takeover control signal procedure.

15. As per claim 17, Stiffler teaches the method further comprising:

wherein said step of changing said state of logical connection, when detecting error occurrence in any of said plurality of physical partitioned computers (primary computer 601 of Fig. 6), inherently updates an allocation table for setting the state of logical connection between said port and each physical partitioned computer, lets said error-detected physical partitioned computer (primary computer) stand by (taken off-line), and activate another physical partitioned computer (secondary computer 603 of Fig. 6) (Fig. 6; Fig. 9; col. 10, ll. 20-49 and col. 11, l. 51 to col. 12, l. 17), wherein upon detection of the primary computer failed, the primary computer is taken off-line and the secondary computer is activated to become the new primary computer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 1, 3, 5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stiffler et al. (US Patent 6,622,263) in view of Pittelkow et al. (US Patent 7,003,688).

17. As per claims 1 and 5, Stiffler teaches a computer system, comprising:

a plurality of physical partitioned computers (Fig. 6, ref. 601, 603) formed by partitioning a computer physically (Fig. 6);

an I/O device (Fig. 6, ref. 616) connected to a PCI bus (Fig. 6, ref. 610, 624) of said computer and shared among said plurality of physical partitioned computers (col. 9, l. 52 to col. 10, l. 10);

a single port disposed in said I/O device and connected to said PCI bus (col. 9, l. 52 to col. 10, l. 10), wherein the disk array (I/O device) is duplicated by having all disk stored initiated on the primary computer echoed by the second computer therefore the disk array would obviously have the single port; and

a PCI connection allocating means for setting a state of logical connection between selected one of said plurality of physical partitioned computers (secondary computer 603 of Fig. 6) and said port (Fig. 9 and col. 10, ll. 20-64); and

I/O device switching means for updating said state of connection set by said PCI connection allocating means according to a control signal received from said selected physical partitioned computer (Fig. 9 and col. 10, ll. 20-64), wherein the secondary computer implement the takeover control signal procedure,

wherein said selected physical partitioned computer (secondary computer) changes its state of logical connection to said I/O device (disk array) according to the setting by said PCI connection allocating means (Fig. 6; Fig. 9 and col. 10, ll. 20-64), wherein the state of logical connection between the secondary computer and the disk array is changed by becoming active.

Stiffler does not expressly teach a computer system comprising wherein the PCI connection allocating means for setting a state of logical connection between selected at most one of said plurality of physical partitioned computers and said port at a time.

Pittelkow teaches a system and method comprising a storage assembly (Fig. 6, ref. 612) connected to a switch (Fig. 6, ref. 608) through a controller (Fig. 6, ref. 610), wherein a plurality of servers (Fig. 6, ref. 602, 604, 606) is coupled to the storage assembly through the switch, wherein said switch and controller enable at most one of said plurality of servers to be connected to the storage assembly at a time (col. 18, ll. 20-56).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Pittelkow's switch and controller into Stiffler's computer system. The resulting combination of the references teach having at most the secondary computer connected to the disk array at a time as the primary computer is taken off-line.

Therefore, it would have been obvious to combine Pittelkow with Stiffler for the benefit of increase the robustness of the interconnection between the disk array and the plurality of computer, because if one of the interconnection were to fail, another interconnection can be established (Pittelkow, col. 18, ll. 41-56).

18. As per claims 3 and 7, Stiffler and Pittelkow teach all the limitations of claims 1 and 5 as discussed above, where Stiffler further teaches the computer system comprising wherein said selected virtual machine (second computer) includes error detecting means for detecting error occurrence in another virtual machine (primary computer) and when such an error is detected, said selected virtual machine (secondary computer) sends a predetermined control signal (takeover control signal procedure) to said I/O device switching means, and said I/O device switching means disables (take off-line) an access of the error occurred virtual machine (primary computer) to said I/O device (Stiffler, Fig. 9 and col. 10, ll. 20-64).

19. Claims 2, 4, 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stiffler et al. (US Patent 6,622,263) and Pittelkow et al. (US Patent 7,003,688), and further in view of "Computer Input/Output".

20. As per claims 2 and 6, Stiffler and Pittelkow teach all the limitations of claims 1 and 5 as discussed above, where Stiffler further teaches the computer system comprising wherein said I/O device switching includes interrupting means for updating the setting by said PCI connection allocating means (Stiffler, Fig. 9 and col. 10, ll. 20-64), wherein the I/O device would be setup to communicate with the secondary computer and stop communication with the primary computer; and

wherein said selected virtual machine changes its state of logical connection to said I/O device according to the setting by said PCI connection allocating means (Stiffler, Fig. 9 and col. 10, ll. 20-64), wherein the state of logical connection between the disk array and the primary computer is deactivated and the state of logical connection between the disk array and the secondary computer is activated.

Stiffler and Pittelkow does not expressly teach the computer system comprising wherein said I/O device switching includes interrupting means for generating an interruption to notify said selected virtual machine of a change of said state of logical connection to said I/O device, and

wherein said selected virtual machine changes its state of logical connection to said I/O device when receiving said interruption.

"Computer Input/Output" teaches the Interrupt Driven I/O (Section 4), wherein the sequence of events is as follows:

the I/O module (I.O device) interrupts the CPU;

the CPU (computer) finishes executing the current instruction;

the CPU acknowledges the interrupt;

the CPU saves its current state; and

the CPU jumps to a sequence of instructions which will handle the interrupt (Section 4).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Computer Input/Output's interrupt into Stiffler and Pittelkow's computer system. The resulting combination of the references teaches further comprising generation of the interrupt signal by the disk array when the disk array receives the takeover control signal procedure from the secondary computer and when the primary and secondary computers receive the disk array's interrupt, the state of logical connection between the primary computer and the disk array is deactivated as the primary computer will be taken off-line and the state of logical connection between the secondary computer and the disk array is activated as the secondary computer takes over to commence operating as the new primary computer.

Therefore, it would have been obvious to combine Computer Input/Output with Stiffler and Pittelkow because not only is the utilization of interrupt signals within the computer system well known, this also provide the benefit of the CPU not to continually poll input devices to see if it must read any data.

21. As per claims 4 and 8, Stiffler, Pittelkow and "Computer Input/Output" teach all the limitations of claims 2 and 6 as discussed above, where Stiffler further teaches the computer system comprising:

wherein first (Stiffler, primary computer 601 of Fig. 6) and second (Stiffler, secondary computer 603 of Fig. 6) physical partitioned computers are included in said plurality of physical partitioned computers (Stiffler, Fig. 6),

wherein said error detecting means, when detecting an error in said first physical partitioned computer (primary computer), sends a predetermined control signal to said I/O device switching means and connects said port of said I/O device to said second physical partitioned computer (Stiffler, col. 10, ll. 20-64), wherein the secondary computer detect the error with the primary computer and implement the takeover control signal procedure for the I/O device and connects to the I/O device operating as the primary computer, and

wherein said computer activates said second virtual machine and lets said first virtual machine stand by (Stiffler, col. 10, ll. 20-64), wherein the secondary computer become active and operating as the new primary computer while the failed primary computer is taken off-line.

22. Claims 9-12, 14 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stiffler et al. (US Patent 6,622,263) in view of "Computer Input/Output".

23. As per claim 9, Stiffler teaches an I/O device (disk array 616 of Fig. 6) connected to a PCI bus of a computer (primary computer 601 and secondary computer 603 of Fig. 6), comprising:

a single port connected to said PCI bus (Fig. 6 and col. 10, ll. 20-64), wherein the disk array is duplicated by having all disk stored initiated on the primary computer echoed by the second computer therefore the disk array would obviously have the single port;

change the state of logical connection of said port according to a control signal received from said computer (Fig. 6 and col. 10, ll. 20-64), wherein when the secondary computer detect error with the primary computer, the secondary computer implement the takeover control signal procedure to change the state of logical connection between the primary computer and the disk array by having the primary computer taken off-line; and

wherein said computer changes its state of logical connection to said port (Fig. 6 and col. 10, ll. 20-64), wherein upon the secondary computer implementing the takeover control signal procedure, the state of logical connection between the primary computer and the disk array is deactivated as the primary computer will be taken off-line and the state of logical connection between the secondary computer and the disk array is activated as the secondary computer takes over to commence operating as the new primary computer.

Stiffler does not expressly teach the I/O device connected to the PCI bus of the computer, comprising:

signal generating means for generating an interruption signal used to change the state of logical connection of said port according to a control signal received from said computer; and

when receiving said interruption signal said computer changes its state of logical connection to said port.

"Computer Input/Output" teaches the Interrupt Driven I/O (Section 4), wherein the sequence of events is as follows:

the I/O module (I/O device) interrupts the CPU;

the CPU (computer) finishes executing the current instruction;

the CPU acknowledges the interrupt;

the CPU saves its current state; and

the CPU jumps to a sequence of instructions which will handle the interrupt (Section 4).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Computer Input/Output's interrupt signal into Stiffler's computer system. The resulting combination of the references teaches further comprising generation of the interrupt signal by the disk array when the disk array receives the takeover control signal procedure from the secondary computer and when the primary and secondary computers receive the disk array's interrupt, the state of logical connection between the primary computer and the disk array is deactivated as

the primary computer will be taken off-line and the state of logical connection between the secondary computer and the disk array is activated as the secondary computer takes over to commence operating as the new primary computer.

Therefore, it would have been obvious to combine Computer Input/Output with Stiffler because not only is the utilization of interrupt signals within the computer system well known, this also provide the benefit of the CPU not to continually poll input devices to see if it must read any data.

24. As per claim 10, Stiffler and "Computer Input/Output" teach all the limitations of claim 9 as discussed above, where both further teach that the system comprising:

wherein said computer includes first (Stiffler, secondary computer 601 of Fig. 6) and second (Stiffler, primary computer 603 of Fig. 6) virtual machines formed therein (Stiffler, Fig. 6),

wherein said signal generating means sends the interruption signal to said second virtual machine (primary computer) to change said state of logical connection of said port to said first virtual machine (secondary computer) according to a control signal received from said first virtual machine (primary computer) (Stiffler, Fig. 6 and col. 10, ll. 20-64 and "Computer Input/Output", section 4), wherein upon the disk array receiving the takeover control signal procedure from secondary computer and generating the interrupt to disable communication with the primary computer as the secondary computer takeover the communication by becoming active and operating as the new primary computer.

25. As per claim 11, Stiffler and "Computer Input/Output" teach all the limitations of claim 9 as discussed above, where both further teach that the system comprising:

comprising an allocating mean for setting said state logical connection of said port (Stiffler, Fig. 6 and col. 10, ll. 20-64), wherein the state of logical connection between the primary computer and the disk array is set to be deactivated and the state of logical connection between the secondary computer and the disk array is set to be activated.

wherein said signal generating means generates an interruption signal and updates said allocating means for setting said state of logical connection of said port (Stiffler, Fig. 6 and col. 10, ll. 20-64 and "Computer Input/Output", section 4), wherein the disk array generate the interrupt signal and update the state of logical connection between the primary computer and the disk array to be deactivated and update the state of logical connection between the secondary computer and the disk array to be activated.

26. As per claim 12, Stiffler teaches an I/O device (disk array 616 of Fig. 6) connected to a plurality of physical partitioned computers (Fig. 6, ref. 601, 603) through a PCI bus (Fig. 6, ref. 610, 624), comprising:

a single port connected to said PCI bus (col. 9, l. 52 to col. 10, l. 10), wherein the disk array (I/O device) is duplicated by having all disk stored initiated on the primary

computer echoed by the second computer therefore the disk array would obviously have the single port; and

changing the state of logical connection between said port to a first physical partitioned computer (secondary computer) according to a control signal (takeover control signal procedure) received from said first physical partitioned computer (secondary computer) included in said plurality of physical partitioned computers (col. 10, ll. 20-64), wherein when the secondary computer generated the takeover control signal procedure, the state of logical connection between the disk array and the secondary computer is activated.

Stiffler does not expressly teach the system comprising signal generating means for sending an interruption signal to said second physical partitioned computer to change a state of logical connection of said port to a first physical partitioned computer according to a control signal received from said first physical partitioned computer included in said plurality of physical partitioned computers.

"Computer Input/Output" teaches the Interrupt Driven I/O (Section 4), wherein the sequence of events is as follows:

the I/O module (I/O device) interrupts the CPU;

the CPU (computer) finishes executing the current instruction;

the CPU acknowledges the interrupt;

the CPU saves its current state; and

the CPU jumps to a sequence of instructions which will handle the interrupt (Section 4).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Computer Input/Output's interrupt signal into Stiffler's computer system. The resulting combination of the references teaches further comprising generation of the interrupt signal by the disk array when the disk array receives the takeover control signal procedure from the secondary computer and when the primary and secondary computers receive the disk array's interrupt, the state of logical connection between the primary computer and the disk array is deactivated as the primary computer will be taken off-line and the state of logical connection between the secondary computer and the disk array is activated as the secondary computer takes over to commence operating as the new primary computer.

Therefore, it would have been obvious to combine Computer Input/Output with Stiffler because not only is the utilization of interrupt signals within the computer system well known, this also provide the benefit of the CPU not to continually poll input devices to see if it must read any data.

27. As per claim 14, Stiffler teaches all the limitations of claim 13 as discussed above. Stiffler further teaches the system comprising wherein said step of changing said state of logical connection includes a step of changing said state of logical connection between said port and said selected virtual machine (Fig. 6 and col. 10, ll. 20-64), wherein the state of logical connection between the primary computer and the disk array is deactivated and the state of logical connection between the secondary computer and the disk array is activated.

Stiffler does not teach the system comprising:

generating an interruption to notify said selected virtual machine of a change of said state of logical connection of said I/O device; and

a step of enabling said selected virtual machine that receives said interruption to change said state of logical connection to said I/O device according to said setting of said state of logical connection.

"Computer Input/Output" teaches the Interrupt Driven I/O (Section 4), wherein the sequence of events is as follows:

the I/O module (I/O device) interrupts the CPU;

the CPU (computer) finishes executing the current instruction;

the CPU acknowledges the interrupt;

the CPU saves its current state; and

the CPU jumps to a sequence of instructions which will handle the interrupt (Section 4).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Computer Input/Output's interrupt signal into Stiffler's computer system. The resulting combination of the references teaches further comprising generation of the interrupt signal by the disk array when the disk array receives the takeover control signal procedure from the secondary computer and when the primary and secondary computers receive the disk array's interrupt, the state of logical connection between the primary computer and the disk array is deactivated as the primary computer will be taken off-line and the state of logical connection between

the secondary computer and the disk array is activated as the secondary computer takes over to commence operating as the new primary computer.

Therefore, it would have been obvious to combine Computer Input/Output with Stiffler because not only is the utilization of interrupt signals within the computer system well known, this also provide the benefit of the CPU not to continually poll input devices to see if it must read any data.

28. As per claim 18, Stiffler teaches a method for sharing an I/O device (disk array 616 of Fig. 6) connected to a PCI bus (Fig. 6, ref. 610, 624) of a computer among a plurality of virtual machines (Fig. 6, ref. 601, 603), wherein said method includes:

a step of enabling said I/O device (disk array) connected to said PCI bus through its single port to change the state of logical connection of said port according to a control signal received from any selected one of said plurality of virtual machines (secondary computer); and a step of changing said state of logical connection between said port and said selected virtual machine (secondary computer) accordingly (Fig. 6; col. 9, l. 52 to col. 10, l. 10 and col. 10, ll. 20-64), wherein the disk array (I/O device) is duplicated by having all disk stored initiated on the primary computer echoed by the second computer therefore the disk array would obviously have the single port and wherein upon receiving the takeover control signal procedure from the secondary computer the state of logical connection between the disk array and the primary computer is deactivated as the primary computer is taken off-line and the state of logical

connection between the disk array and the secondary computer is activated as the secondary computer commence to operate as the new primary computer.

Stiffler does not expressly teaches the system comprising a step of enabling said I/O device to generate an interruption signal used to change the state of logical connection; and a step of changing said state of logical connection between said port and said selected virtual machine according to said received interruption signal.

"Computer Input/Output" teaches the Interrupt Driven I/O (Section 4), wherein the sequence of events is as follows:

the I/O module (I/O device) interrupts the CPU;

the CPU (computer) finishes executing the current instruction;

the CPU acknowledges the interrupt;

the CPU saves its current state; and

the CPU jumps to a sequence of instructions which will handle the interrupt (Section 4).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Computer Input/Output's interrupt signal into Stiffler's computer system. The resulting combination of the references teaches further comprising generation of the interrupt signal by the disk array when the disk array receives the takeover control signal procedure from the secondary computer and when the primary and secondary computers receive the disk array's interrupt, the state of logical connection between the primary computer and the disk array is deactivated as the primary computer will be taken off-line and the state of logical connection between

the secondary computer and the disk array is activated as the secondary computer takes over to commence operating as the new primary computer.

Therefore, it would have been obvious to combine Computer Input/Output with Stiffler because not only is the utilization of interrupt signals within the computer system well known, this also provide the benefit of the CPU not to continually poll input devices to see if it must read any data.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C.K.L.
05/02/2006

Supervisory Patent Examiner

ftz m. fleming

FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100

5/8/2006

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